REMARKS

Claims 37-55 were prending and rejected. In response, Applicant has cancelled claims 45 and 51 (without prejudice), amended claims 37, 43-44, 46-47, 50, and 52-55, and added new claim 56. No new matter has been introduced. Accordingly, claims 37-44, 46-50 and 52-56 are pending, and reconsideration is respectfully requested.

In the subject Office Action, the Examiner rejected claims 37-39, 43-48 and 50-55 under 35 USC §102(b) as being anticipated by Requa. The Examiner asserted each of the recitations is fully anticipated. Applicant respectfully disagree. However, in the interest of furthering prosecution, Applicant has nonetheless amended the claims and the claims are clearly patentable over the cited reference.

In particular, claim 37 has been amended to recite

> assigning a group of instructions selected from the plurality of groups of instructions partitioned from the program to a plurality of interconnected preselected computation nodes;
>
> loading a subset of instructions of the assigned group of instructions into a frame of buffers spanning the plurality of interconnected preselected computation nodes having been assigned the group of instructions; and
>
> executing the subset of instructions as each one of the instructions in the subset of instructions loaded into the frame of spanning buffers receives all necessary associated operands for execution.

As the Examiner has argued in multiple places in the Office Action, Requa teaches issuing each instruction of a group of instruction to one of a plurality of processors to execute, and the claim language can be read on Requa. Since Requa teaches issuing each instruction to a processor to execute, it is plain then the reference does not teach or anticipate "loading a subset of instructions of the assigned group of instructions into a frame of buffers spanning the plurality of interconnected preselected computation nodes having been assigned the group of instructions," and then "executing the subset of instructions as each one of the instructions in the subset of instructions loaded into the frame of spanning buffers receives all necessary associated operands for execution."

Accordingly, for at least these reasons, claim 37 is patentable over the cited reference.

Claim 47 includes similar recitation as discussed above for claim 37, and therefore is also patentable over the cited reference for reasons at least similar to the reasons discussed for claim 37.

Claims 38-44, 46, 48-50, and 52-56 depend from claims 37 and 47 incorporating their recitations. Therefore, for at least the same reasons, claims 38-44, 46, 48-50, and 52-56 are patentable over the cited reference.

Claims 38-44, 38-44, 46, 48-50, and 52-56 are further patentable over the cited reference because of their additional recitations, in particular, the recitations amended to reference "the frame of buffers spanning the plurality of interconnected preselected computation nodes," in e.g. claims 43-44 and 46-47, and the recitations associated with "repeating said loading (and executing) until the entire group of instructions are executed" in e.g. claims 53-54 and 56.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,
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